

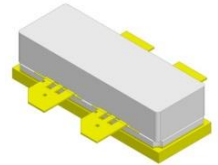


Product Features

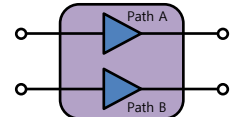
- 2300~2500MHz
- 347W Saturated Power @ 48V
- Peak Power 55.4dBm@2400MHz
- Internally Matched
- Asymmetrical Doherty GaN HEMT
- Excellent Thermal Stability

Applications

- Plasma Lighting System
- RF Heating and Drying
- Solid state Microwave OVEN
- Semiconductor Equipment
- Bio & Health Sciences



Package Type : RF18010DKR3



Typical Single-Carrier LTE Performance $(V_{DS} = +48V, T_C = 25^\circ C, 50\Omega)$

Frequency [MHz]	Peak Power	Average Power ^{*1}			
	Power [W]	Input Power [W]	Gain [dB]	Drain Efficiency [%]	ACLR [dBc]
2400.0	343.1	15	13.6	47.9	-30.4
2450.0	338.2	15	13.5	47.2	-33.2
2500.0	332.5	15	13.5	46.4	-33.2

Note

*1 Measured in the ID24330WD Doherty test board amplifier circuit, under LTE 10MHz, PAR 7.5dB @0.01% probability on CCDF

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Condition
Drain to Source Voltage	V_{DSS}	150	V	$T_C = 25^\circ C$
Gate to Source Voltage	V_{GS}	-10, +2	V	$T_C = 25^\circ C$
Operating Voltage	V_{DD}	52	V_{DC}	
Storage Temperature	T_{STG}	-65, +150	$^\circ C$	
Case Operating Temperature	T_C	-40, +150	$^\circ C$	
Operating Junction Temperature ^{*1}	T_J	225	$^\circ C$	
Soldering Temperature ^{*2}	T_S	245	$^\circ C$	

Note

*1 Continuous use at maximum temperature will affect MTF.

*2 Refer to the Application Note(AN-002) on soldering - "Solder Condition for RFHIC's GaN Device"

Thermal Characteristics

Rating	Symbol	Value	Unit	Condition
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2.14 ^{*1}	$^\circ C/W$	$T_C = 85^\circ C$

Note

*1 Measured for the ID24330WD at dissipation power is 65W.

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC Characteristics - Path A (Carrier)^{*1}						
Maximum Forward Gate Current	$T_C= 25^\circ\text{C}$	I_{GMAX}	-	-	16	mA
Maximum Drain Current ^{*2}	$T_C= 25^\circ\text{C}$	I_{DMAX}	-	-	6.0	A
Power Dissipation	$T_C= 85^\circ\text{C}$	P_{DMAX}	-	-	65	W
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ $I_D = 14.4\text{mA}$	$V_{GS(TH)}$	-3.75	-3.00	-2.25	V_{DC}
Gate Quiescent Voltage	$V_{DS} = 48\text{V}$ $I_D = 200\text{mA}$	$V_{GS(Q)}$	-	-2.85	-	V_{DC}
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ $I_D = 14.4\text{mA}$	V_{BR}	150	-	-	V
Saturated Drain Current ^{*3}	$V_{DS} = 6\text{V}$ $V_{GS} = 2\text{V}$	I_{DS}	12.0	14.4	-	A
Gate Leakage Current	$V_{GS} = -8\text{V}$ $V_{DS} = 150\text{V}$	$I_{GLKG150}$	-3.3	-	-	mA
Drain Leakage Current	$V_{GS} = -8\text{V}$ $V_{DS} = 150\text{V}$	$I_{DLKG150}$	-	-	5.8	mA
DC Characteristics - Path B (Peaking)^{*1}						
Maximum Forward Gate Current	$T_C= 25^\circ\text{C}$	I_{GMAX}	-	-	24	mA
Maximum Drain Current ^{*2}	$T_C= 25^\circ\text{C}$	I_{DMAX}	-	-	9.0	A
Power Dissipation	$T_C= 85^\circ\text{C}$	P_{DMAX}	-	-	80.0	W
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ $I_D = 21.6\text{mA}$	$V_{GS(TH)}$	-3.75	-3.00	-2.25	V_{DC}
Gate Quiescent Voltage	$V_{DS} = 48\text{V}$ $I_D = 750\text{mA}$	$V_{GS(Q)}$	-	-2.700	-	V_{DC}
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ $I_D = 21.6\text{mA}$	V_{BR}	150	-	-	V
Saturated Drain Current ^{*3}	$V_{DS} = 6\text{V}$ $V_{GS} = 2\text{V}$	I_{DS}	18.0	21.6	-	A
Gate Leakage Current	$V_{GS} = -8\text{V}$ $V_{DS} = 150\text{V}$	$I_{GLKG150}$	-4.5	-	-	mA
Drain Leakage Current	$V_{GS} = -8\text{V}$ $V_{DS} = 150\text{V}$	$I_{DLKG150}$	-	-	5.8	mA

Note

*1 Measured on wafer prior to packaging.

*2 Current Limit for long term, reliable operation

*3 Scaled from PCM data.

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
RF Characteristics (F=2450MHz unless otherwise noted)						
Saturated Output Power ^{*1,4}	V_{DS} = 48V	P _{SAT}	200	347	-	W
	I_{DQ} = 200mA					
Modulated Gain ^{*2}	V_{DS} = 48V	G _{BR}	12.5	13.5	-	dB
	I_{DQ} = 200mA					
	P_{OUT} = 46.8dBm					
LTE Linearity ^{*2}	V_{DS} = 48V	ACLR	-	-24.0	-22.0	dBc
	I_{DQ} = 200mA					
	P_{OUT} = 46.8dBm					
Modulated Drain Efficiency ^{*2}	V_{DS} = 48V	η	43	48	-	%
	I_{DQ} = 200mA					
	P_{OUT} = 46.8dBm					
Output Mismatch Stress ^{*1,3}	V_{DS} = 48V	VSWR	-	-	10:1	ψ
	I_{DQ} = 200mA					
	P_{OUT} = P_{SAT} Pulsed					

Note

*1 Pulse width 100μsec, Duty Cycle 10%.

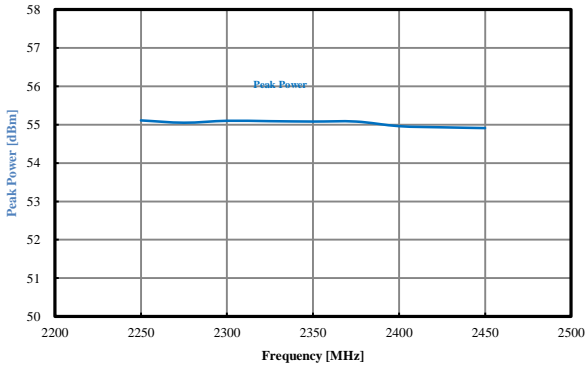
*2 Measured in the ID24330WD Doherty test board amplifier circuit, under LTE 10MHz, PAR7.5dB @0.01% probability on CCDF.

*3 Measured in the ID24330WD Doherty test board amplifier circuit. No damage at all phase angles.

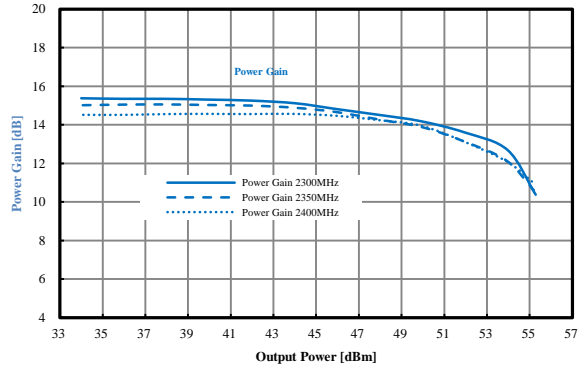
*4 Psat is defined as $\Delta P_{out}/\Delta P_{in} < 0.1$, where ΔP_{in} is increased input power, ΔP_{out} is increased output power.

Typical Pulsed Signal Performance (Tc=25°C, Measured in the ID24330WD test board amplifier circuit)

Peak Power vs. Frequency



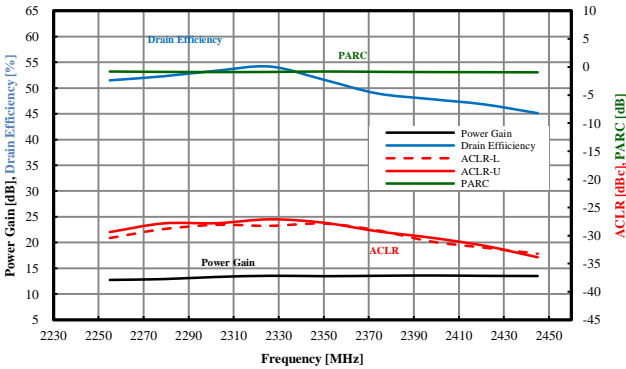
Pulsed Power Gain vs. Output Power



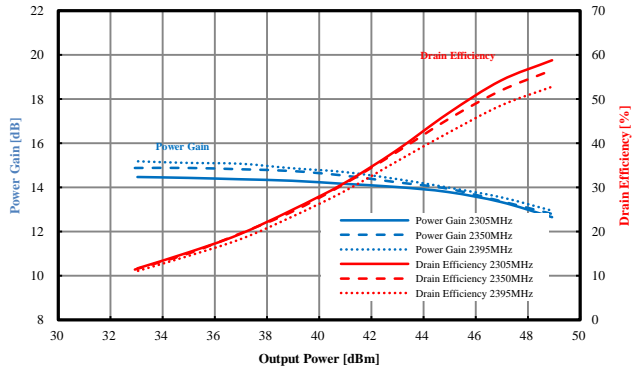
$V_{DS} = 48V$, $I_{DQ(C)} = 200mA$, $V_{GS(P)} = -5.5V$, Pulse Width = 100µsec, Duty Cycle = 10%

Typical LTE Signal Performance (Tc=25°C, Measured in the ID24330WD test board amplifier circuit)

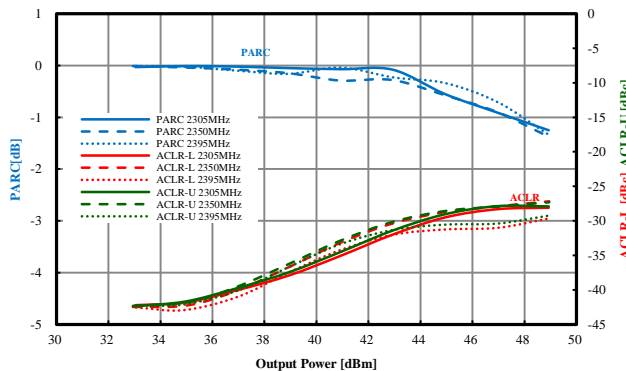
LTE Power Gain, Drain Efficiency, ACLR, PARC vs. Frequency



Power Gain, Drain Efficiency vs. Output Power



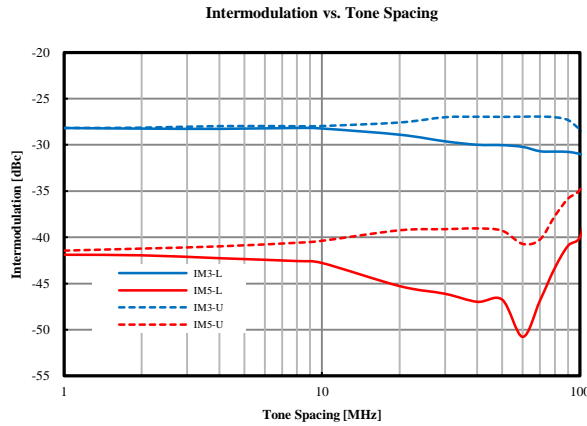
PARC, ACLR vs. Output Power



$P_{AVG} = 46.8dBm$, $V_{DS} = 48V$, $I_{DQ(C)} = 200mA$, $V_{GS(P)} = -5.5V$
LTE 10MHz BW, PAPR=7.5dB @ 0.01% Probability on CCDF

Typical 2-tone Intermodulation Imbalance Performance

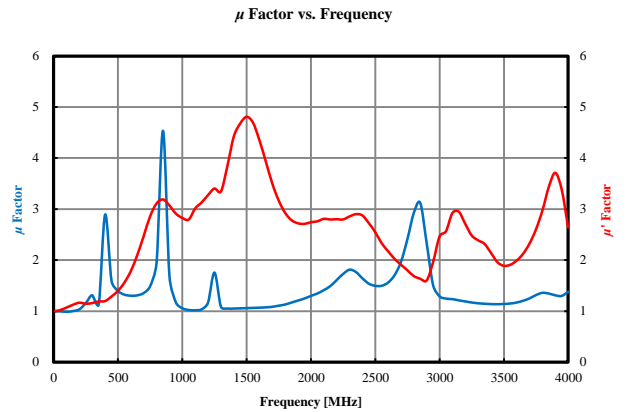
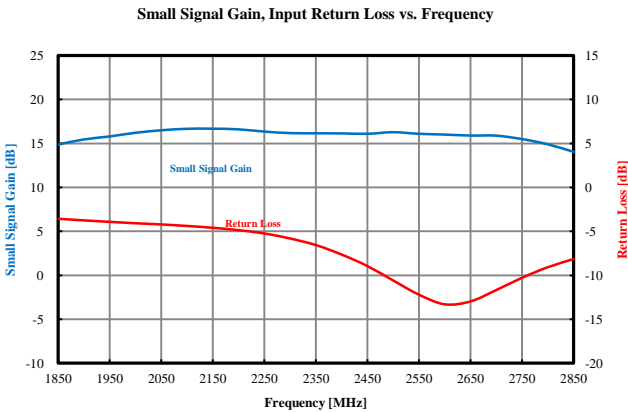
(Tc=25°C, Measured in the ID24330WD Doherty test board amplifier circuit)



2-tone Power = 46.8dBm, $V_{DS} = 48V$, $I_{DQ(C)} = 200mA$, $V_{GS(P)} = -5.5V$

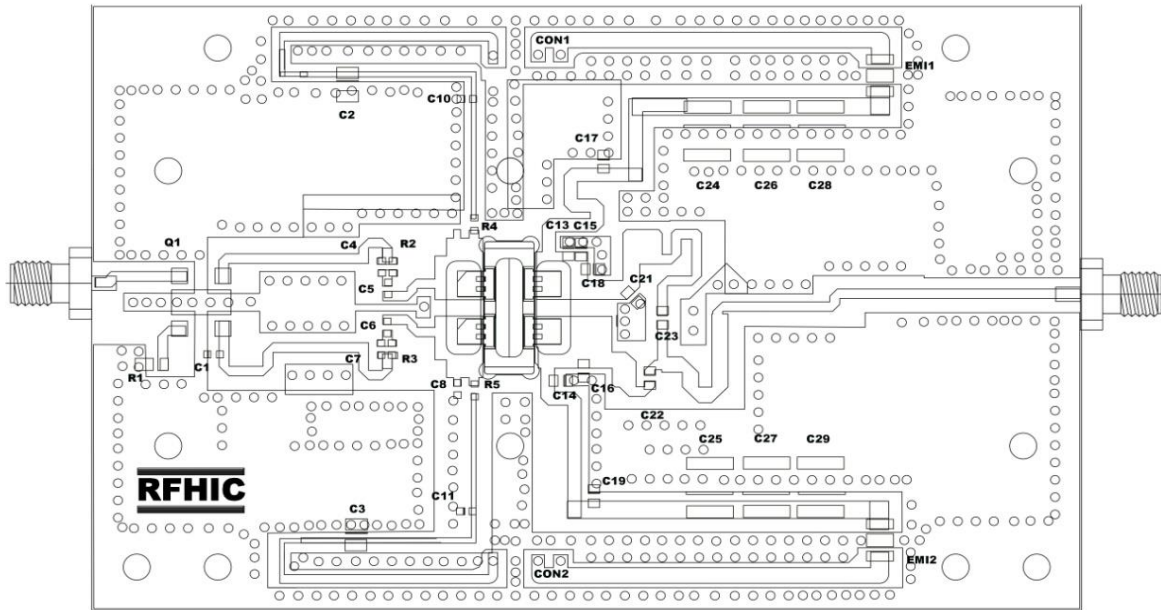
Typical Small Signal Performance

(Tc=25°C, Measured in the ID24330WD Doherty test board amplifier circuit)



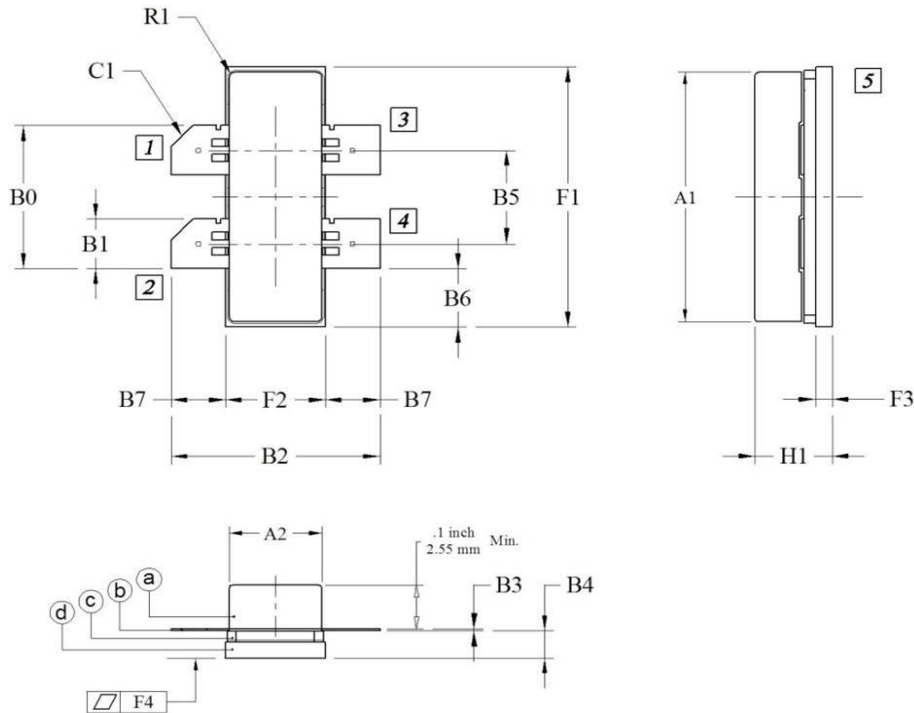
$P_{IN} = 0dBm$, $V_{DS} = 48V$, $I_{DQ} = 200mA$, $V_{GS(P)} = -5.5V$

Test Board Component Layout



Part	Description	Part Number	Manufacturer
R1	50 ohm Term	S1020A	RN2
R2, R3	5.1 ohm Chip Resistor	MCR10EZPJ5R1	ROHM
R4, R5	10 ohm Chip Resistor	MCR10EZPJ100	ROHM
C1	0.5 pF High Q Capacitor, 1608	GQM1875C2E0R5GB12D	MURATA
C2, C3	4.7 uF High Q Capacitor, 3225	GRM32ER72A475KA,3225,100V	MURATA
C4,C5,C6,C7,C10,C11	8.2 pF High Q Capacitor, 1608	GQM1875C2E8R2BB12D	MURATA
C8	1.2pF High Q Capacitor, 1608	GRM32ER72A225KA,3225,100V	MURATA
C13, C15	1.8pF High Q Capacitor, 2012	GQM2195C2E1R8BB12D	MURATA
C14, C18	1.0pF High Q Capacitor, 2012	GQM2195C2E1R0BB12D	MURATA
C16	1.2pF High Q Capacitor, 2012	GQM2195C1E2R3BB12D	MURATA
C17, C19, C22	6.8pF High Q Capacitor, 2012	GQM2195C2E6R8BB12D	MURATA
C21	0.5pF High Q Capacitor, 2012	GQM2195C2E0R5BB12D	MURATA
C24,C25,C26,C27,C28,C29	10uF MLCC	RS80R2A106M, 5750, 100V	MARUWA
Q1	2.3~2.7 GHz Hybrid coupler	1P603AS	ANAREN
EMI1, EMI2	EMI FILTER	CTH32R102S20A-TM	MARUWA
CON1, CON2	DC Connector, 4 Pin	5267-04A	MOLEX
PCB	$\epsilon_r=3.66 \pm 0.05, 0.020'' (0.508mm)$	RO4350B	ROGERS Corp.
TR1	275W GaN Transistor	ID24300WD	RFHIC

Package Dimensions (Type:RF18010DKR3)

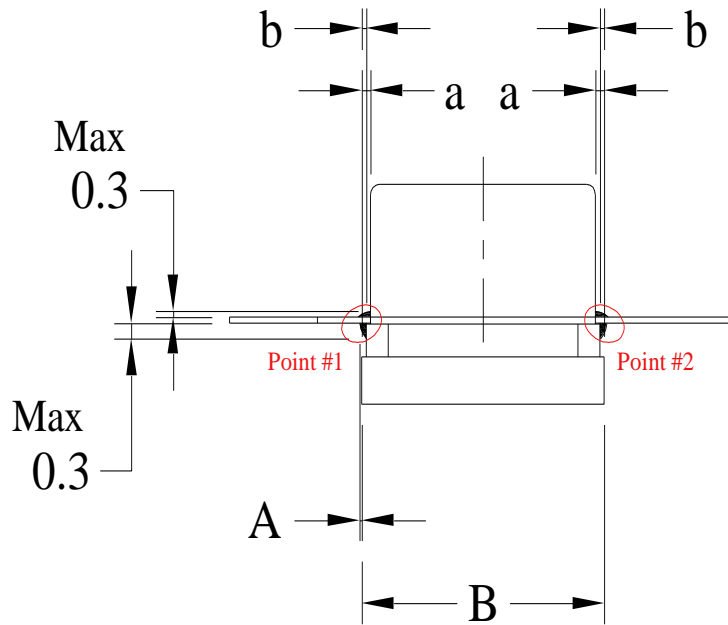


Pin Description	
Pin No	Function
1	Path A Gate
2	Path B Gate
3	Path A Drain
4	Path B Drain
5	Source

- Ⓐ- Lid
- Ⓑ- Lead Frame
- Ⓒ- Ceramic Ring
- Ⓓ- Flange

Dim.	INCH			MILLIMETER		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	.573	.579	.585	14.55	14.70	14.85
A2	.195	.201	.207	4.95	5.10	5.25
B0	.325	.331	.337	8.25	8.40	8.55
B1	.109	.114	.119	2.775	2.900	3.025
B2	.432	.453	.473	10.98	11.50	12.03
B3	.003	.005	.007	0.075	0.125	0.175
B4	.057	.062	.067	1.455	1.580	1.705
B5	.211	.217	.222	5.35	5.50	5.65
B6	-	.136	-	-	3.45	-
B7	-	.118	-	-	3.00	-
C1 (Chamfer)	.034	.039	.044	0.875	1.000	1.125
F1	.597	.602	.607	15.175	15.300	15.425
F2	.212	.217	.221	5.375	5.500	5.625
F3	.032	.036	.040	0.82	0.92	1.02
F4	-	.002	-	-	0.05	-
H1	.157	.167	.177	4.00	4.25	4.50
R1 (Radius)	.008	.012	.016	0.20	0.30	0.40

Lid Epoxy Tolerance & Package Alignment



Inspection Items	Package Area	Inspection Method
Point#1 (Below the leadframe)	Gate Lead Frame	A: Gate epoxy overflow If 'A' exceeds than 200um or 'A+B' exceeds maximum width of the basemetal, then the product should be rejected..
Point#2 (Below the leadframe)	Drain Lead Frame	B : Package base width If the epoxy overflows the base (B) of package, then the product should be rejected.
a	Ceramic Lid to Basemetal	$a \geq 0$ (a:Distance between ceramic lid edge and basemetal edge)
b	Ceramic Ring to Basemetal	$b \geq 0$ (b:Distance between ceramic ring edge and basemetal edge)

Revision History

Part Number	Release Date	Version	Description	Data Sheet Status
ID24330WD	December, 2021	1.0	Initial release of datasheet	

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