

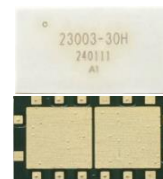
Product Features

- 2300~2400MHz
- 44.7W Saturated Power @ 48V
- 13% Drain Efficiency @ 31dBm
- Internally 50ohm Matched
- 2-Stage Amplifier Module
- GaN on SiC Technology

Applications

- Massive MIMO
- 4G System
- Multi-Band, Multi-Mode
- Multi-Carrier
- RRH Drive Amplifier

RoHS
Compliant



Package Type : PP-3G

Description

The SDM23003-30H is a fully integrated micro-strip GaN Hybrid power amplifier module designed for applications in 4G LTE MIMO systems, small cells and low power remote radio heads. SDM Series is an integrated 2-stage power amplifier module, 50ohm input and output impedance matched device can deliver up to 44.7W of saturation power and operating drain voltage 48V. This device is size 8x14x2.6mm and is packaged in a ceramic surface mount package.

Typical Performance

($V_{DS} = +48V$, $T_C = 25^\circ C$, 50 Ω)

Frequency [MHz]	Peak Output Power	Average Power ^{*1}			
	Power [W]	Power [W]	Gain [dB]	Drain Efficiency [%]	ACLR [dBc]
2310	50.9	1.3	43.3	12.6	-41.9
2350	50.2	1.3	43.6	12.7	-41.6
2390	48.9	1.3	43.9	12.8	-41.8

Note

*1 Measured in the SDM23003-30H test board amplifier circuit, under LTE 20MHz 1carrier, PAR 7.5dB @0.01% probability on CCDF.

Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Condition
Drain to Source Voltage	V_{DSS}	100	V	$T_C = 25^\circ C$
Gate to Source Voltage	V_{GS}	-10, +2	V	$T_C = 25^\circ C$
Operating Voltage	V_{DD}	52	V_{DC}	
Storage Temperature	T_{STG}	-40, +125	$^\circ C$	
Case Operating Temperature	T_C	-30, +125	$^\circ C$	
Operating Junction Temperature ^{*1}	T_J	225	$^\circ C$	
Soldering Temperature ^{*2}	T_S	250	$^\circ C$	

Note

*1 Continuous use at maximum temperature will affect MTTF.

*2 Refer to the Application Note(AN-002) on soldering - "Solder Condition for RFHIC's GaN Device"

Electrical Characteristics^{*1} (T_C=25°C unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC Characteristics (Main)						
Maximum Forward Gate Current	T _c = 25°C	I _{GMAX}	-	-	5	mA
Maximum Drain Current ^{*2}	T _c = 25°C	I _{DMAX}	-	-	3.2	A
Power Dissipation	T _c = 85°C	P _{DMAX}	-	-	29.8	W
Gate Threshold Voltage	V _{DS} = 10V	V _{GS(TH)}	-3.8	-3.0	-2.3	V _{DC}
	I _D = 5.2mA					
Gate Quiescent Voltage	V _{DS} = 48V	V _{GS(Q)}	-3.7	-2.9	-2.2	V _{DC}
	I _D = 60mA					
Drain-Source Breakdown Voltage	V _{GS} = -8V	V _{BR}	150	-	-	V
	I _D = 5.2mA					
Saturated Drain Current ^{*3}	V _{DS} = 6V	I _{DS}	4.2	5.2	-	A
	V _{GS} = 2V					
Gate Leakage Current	V _{GS} = -8V	I _{GLKG150}	-1.6	-	-	mA
	V _{DS} = 150V					
Drain Leakage Current	V _{GS} = -8V	I _{DLKG150}	-	-	2.1	mA
	V _{DS} = 150V					
DC Characteristics (Drive)						
Maximum Forward Gate Current	T _c = 25°C	I _{GMAX}	-	-	1	mA
Maximum Drain Current ^{*2}	T _c = 25°C	I _{DMAX}	-	-	0.3	A
Power Dissipation	T _c = 85°C	P _{DMAX}	-	-	12.2	W
Gate Threshold Voltage	V _{DS} = 10V	V _{GS(TH)}	-3.8	-3.0	-2.3	V _{DC}
	I _D = 0.52mA					
Gate Quiescent Voltage	V _{DS} = 48V	V _{GS(Q)}	-3.7	-2.7	-2.2	V _{DC}
	I _D = 30mA					
Drain-Source Breakdown Voltage	V _{GS} = -8V	V _{BR}	0	-	-	V
	I _D = 0.52mA					
Saturated Drain Current ^{*3}	V _{DS} = 6V	I _{DS}	0.4	0.5	-	A
	V _{GS} = 2V					
Gate Leakage Current	V _{GS} = -8V	I _{GLKG150}	-0.2	-	-	mA
	V _{DS} = 150V					
Drain Leakage Current	V _{GS} = -8V	I _{DLKG150}	-	-	0.2	mA
	V _{DS} = 150V					

Note

*1 Measured on wafer prior to packaging.

*2 Current Limit for long term, reliable operation

*3 Scaled from PCM data.

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
RF Characteristics (F=2350MHz unless otherwise noted)						
Saturated Output Power ^{*1,4}	V_{DS} = 48V	P _{SAT}	35.5	44.7	56	W
Modulated Gain ^{*2}	V_{DS} = 48V	G _p	38	43	48	dB
	P_{OUT} = 31dBm					
Linearity ^{*2}	V_{DS} = 48V	ACLR	-50	-40	-30	dBc
	P_{OUT} = 31dBm					
Modulated Drain Efficiency ^{*2}	V_{DS} = 48V	η	11	13	15	%
	P_{OUT} = 31dBm					
Output Mismatch Stress ^{*1,3}	V_{DS} = 48V	VSWR	-	-	10:1	ψ
	P_{OUT} = P_{SAT} Pulsed					

Note

*1 Pulse width 10μsec, Pulse period 100μsec.

*2 Measured in the SDM23003-30H test board amplifier circuit, under LTE 20MHz 1carrier, PAR 7.5dB @0.01% probability on CCDF.

Drive Idq=30mA, Main Idq=60mA

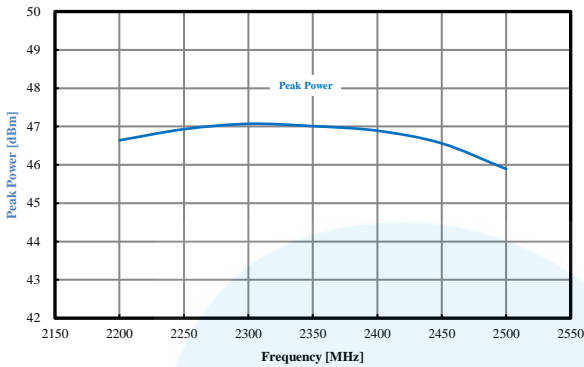
*3 Measured in the SDM23003-30H test board amplifier circuit. No damage at all phase angles.

*4 Psat is defined as $\Delta P_{out}/\Delta P_{in} < 0.1$, where ΔP_{in} is increased input power, ΔP_{out} is increased output power.

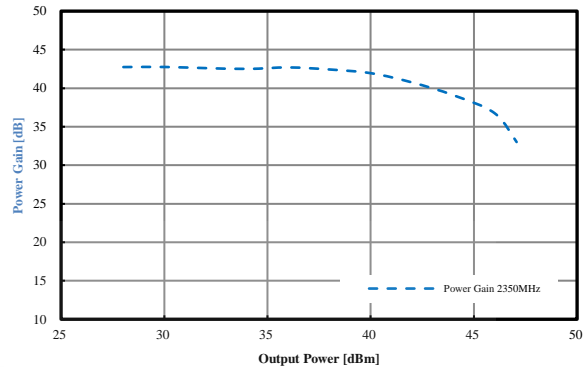
Typical Pulsed Signal Performance

(Tc=25°C, Measured in the SDM23003-30H test board amplifier circuit)

Peak Power vs. Frequency



Pulsed Power Gain vs. Output Power

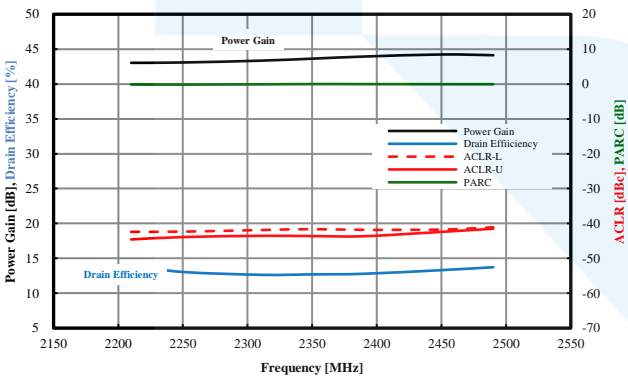


Pulse width 10µsec, Pulse period 100µsec.

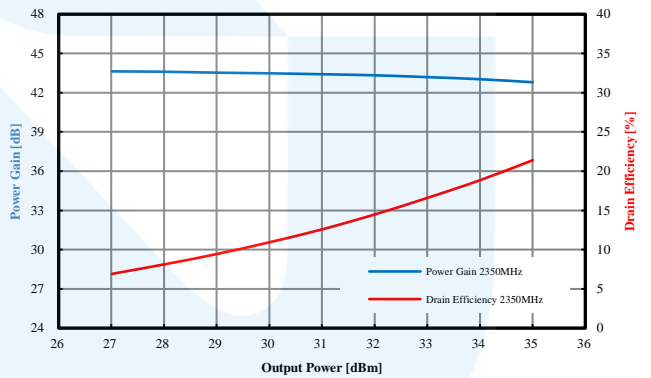
Typical Modulated Signal Performance

(Tc=25°C, Measured in the SDM23003-30H test board amplifier circuit)

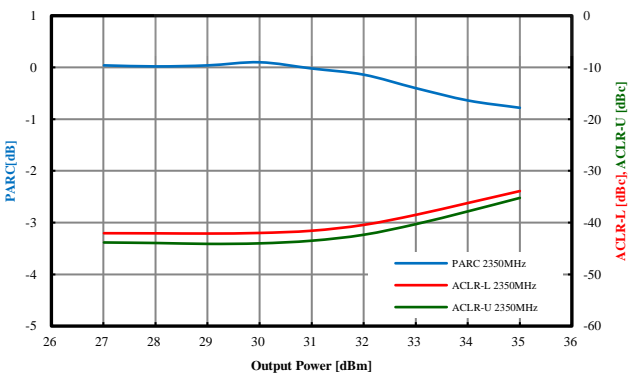
Power Gain, Drain Efficiency, ACLR, PARC vs. Frequency



Power Gain, Drain Efficiency vs. Output Power



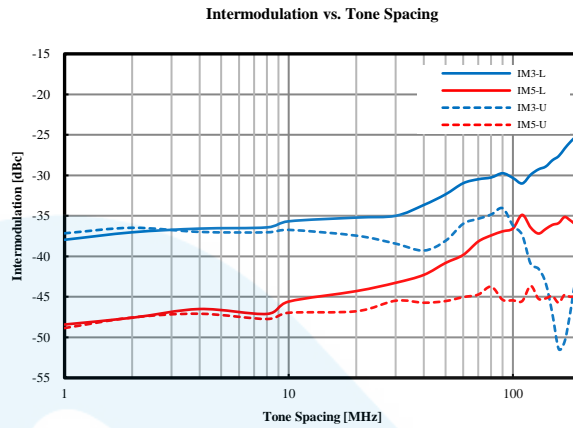
PARC, ACLR vs. Output Power



$P_{AVG} = 31\text{dBm}$, $V_{DS} = 48\text{V}$, Drive Idq=30mA, Main Idq=60mA
 LTE 20MHz 1carrier, PAR 7.5dB @0.01% probability on CCDF.

Typical 2-tone Intermodulation Imbalance Performance

(Tc=25°C, Measured in the SDM23003-30H test board amplifier circuit)



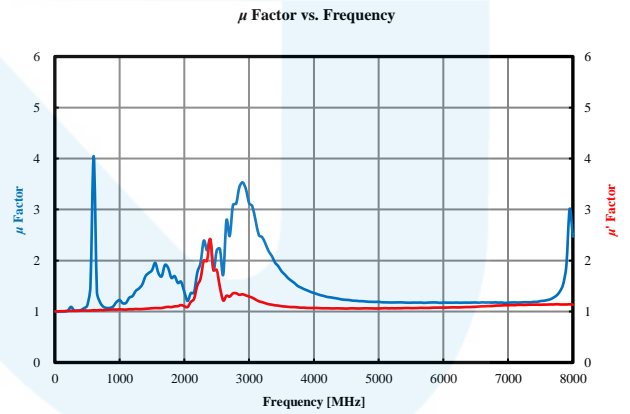
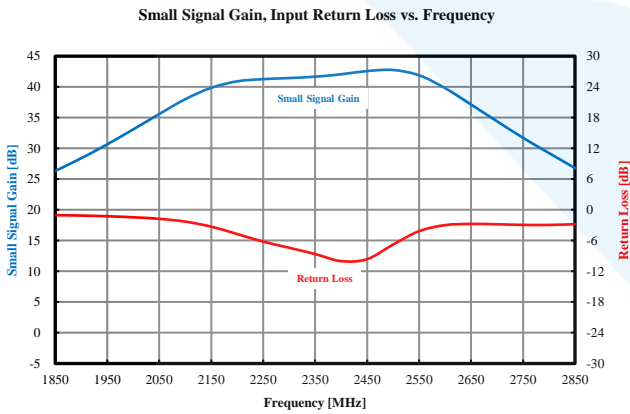
2-tone Power = 31dBm,

$V_{DS} = 48V$,

Drive Idq=30mA, Main Idq=60mA

Typical Small Signal Performance

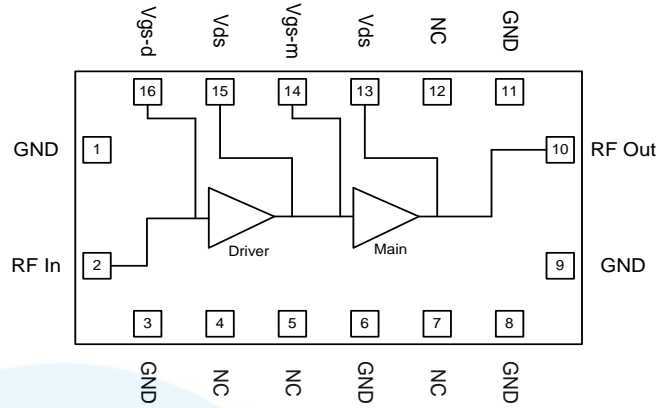
(Tc=25°C, Measured in the SDM23003-30H test board amplifier circuit)



Input Power= -30dBm, $V_{DS} = 48V$,

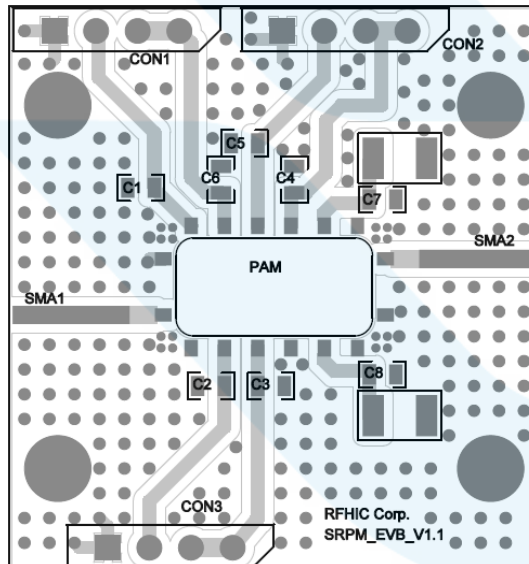
Drive Idq=30mA, Main Idq=60mA

Block Diagram



* Gate Pin assignment
 - Vgs-d (Driver Gate)
 - Vgs-m (Main Gate)

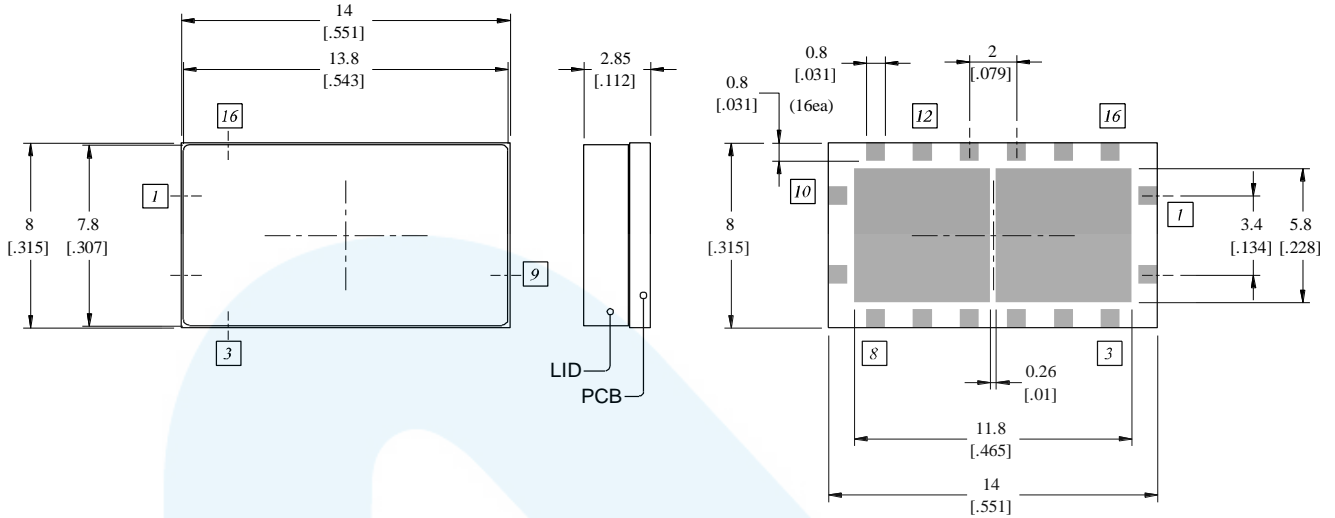
Test Board Component Layout



Part	Description	Part Number	Manufacturer
C3, C4, C6, C7, C8	1.0uF / 100V	GRM21BC72A105KE01	MURATA
C1, C2, C5	4.7uF / 16V	GRM21BR71C475KE51L	MURATA
PCB	2Layer, 20mil, 1oz	RO4350B	ROGERS
CON1~3	2.54mm Male Connector	5267-04A	MOLEX
SMA1~2	Female Connector	-	-
PAM	GaN Hybrid PAM	SDM23003-30H	RFHIC

Package Dimensions (Type:PP-3G)

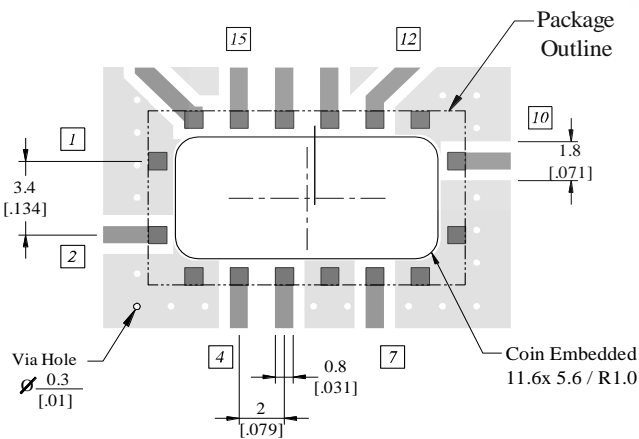
* Unit: mm[inch] | Tolerance: ± 0.15 [.006]



Pin Description								
2	4	5	10	13	14	15	16	7 12
RF In	-	-	RF Out	V _{DS}	V _{GS-m}	V _{DS}	V _{GS-d}	-
-	-	-	-	Main	Main	Drive	Drive	

* Other Pins are GND.

Recommended Footprint & Coin Embedded



ESD Sensitivity Ratings

	ESD Class	Standard
HBM	1A	ANSI/ESDA/JEDEC Standard JS-001
CDM	C1	ANSI/ESDA/JEDEC Standard JS-002

Packing Information

Part Number	Description
SDM23003-30H	600 pcs on a 13" reel (Standard)

Lot Number Description

2	4	0	9	0	1
①	②	③	④	⑤	⑥

- ①② Year Number
- ③④ Week Number
- ⑤⑥ Production Number

Revision History

Part Number	Release Date	Version	Description	Data Sheet Status
SDM23003-30H	Feb, 2024	1.0	Initial Release	



Certification

This product is manufactured by a company that is certified for the AS9100D quality management system.

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